Q.P. Code: 16EC402 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations November-2020

SWITCHING THEORY AND LOGIC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Convert the following numbers. i. (5164.4413)8 to binary ii. Convert (A3C2.D)16 to binary and then to octal. iii. (1032.2)6 to decimal	**6M**
	b	Simplify the following Boolean expressions to minimum no. of literals. i. ABC+A'B+ABC' ii. (BC'+A'D)(AB'+CD') iii. x'yz+xz iv. xy+x(wz+wz')	**6M**

OR

2	**a**	Subtract the given binary numbers 111001-1010 by using 2's complement form.	**6M**
	b	Obtain the Dual of the following Boolean expressions. i. AB+A(B+C)+B' (B+D) ii. A+B+A'B'C iii. A'B+A'BC'+A'BCD+A'BC'D'E iv. ABEF+ABE'F'+**A'B'EF**	**6M**

UNIT-II

3	**a**	Minimize the following Boolean function using K-Map F(A, B, C, D)= Σm (0, 2, 4, 6, 8, 10, 12, 14).	**6M**
	b	Realize the above Boolean function using NAND Gates only.	**6M**

OR

4	**a**	Simplify the Boolean function by using tabulation method F(A, B, C, D)=Σm (0, 1, 2, 5, 6, 7, 8, 9, 10, 14)	**10M**
	b	Implement AND gate using NOR gate(s) only.	**2M**

UNIT-III

5	**a**	Design and implement BCD to Excess-3 code converter using logic gates.	**6M**
	b	Design 32:1 Multiplexer using two 16:1 Muxs and one 2:1 Mux using block diagram representation.	**6M**

OR

6	**a**	Design the full adder circuit using half adders	**6M**
	b	Draw and explain the operation of 3×2 binary multiplier.	**6M**

UNIT-IV

7	**a**	Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram neatly.	**6M**
	b	A clocked sequential circuit with single input x and single output z produces an output z =1 whenever the input x compares the sequence 1011 and overlapping is allowed. Obtain the state diagram, state table and design the circuit with D flip-flops.	**6M**

OR

8	**a**	Design a binary counter having repeated binary sequence 0, 1, 2, 4, 5, 6 using JK flip flops.	**6M**
	b	Implement 4-bit ring counter using suitable shift register. Briefly describe its operation.	**6M**

UNIT-V

9	**a**	Implement the following two Boolean functions with a PLA: F1(A, B, C) = Σ(0, 1, 2, 4) F2(A, 3, C) = Σ (0, 5, 6, 7)	**6M**
	b	Discuss briefly about Mealy models of sequential machines.	**6M**

OR

10		Implement the following Boolean functions with a PAL: W(A,B,C,D)= Σ(2,12,13) X(A,B,C,D)= Σ(7,8,9,10,11,12,13,14,15) Y(A,B,C,D)= Σ(0,2,3,4,5,6,7,8,10,11,15) Z(A,B,C,D)= Σ(1,2,8,12,13)	**12M**

*** END ***